Claims:

1. A high-density circuit module comprising:

a first CSP having first and second major surfaces and a first and a second edge, the edges delineating a lateral extent for the upper major surface;

a second CSP;

a form standard disposed between the first and second CSPs, the form standard having a lateral extent greater than the lateral extent of the upper major surface of the first CSPs;

a flex circuit connecting the first and second CSPs and disposed to place a first portion of the flex circuit beneath the lower major surface of the first CSP and a second portion of the flex circuit above the form standard disposed between the first and second CSPs.

2. The high-density circuit module of claim 1 in which the flex circuit comprises:

first and second conductive layers, between which there is an intermediate layer, the second conductive layer having demarked first and second flex contacts, the first flex contacts in electrical connection with the first CSP and the second flex contacts in electrical connection with the second CSP.

3. The high-density circuit module of claim 1 in which the flex circuit comprises a conductive layer that expresses first and second flex contacts for connection of the first and second CSPs.

4. A high-density circuit module comprising:

a first flex circuit having first and second flex contacts;

a second flex circuit having first and second flex contacts;

a first CSP having CSP contacts, the CSP contacts of the first CSP contacting the first flex contacts of each of the first and second flex circuits;

a form standard disposed between the first and second CSPs;

a second CSP having CSP contacts, the first CSP being disposed above the form standard and the second CSP and the CSP contacts of the second CSP contacting the second flex contacts of each of the first and second flex circuits.

5. A high-density circuit module comprising:

a first flex circuit having first and second flex contacts;

a second flex circuit having first and second flex contacts;

a first CSP having CSP contacts in contact with the second flex contacts of each of the first and second flex circuits;

a form standard disposed between the first and second CSPs;

a second CSP having CSP contacts, the first CSP being disposed above the form standard and the second CSP and the CSP contacts of the second CSP contacting the first flex contacts of each of the first and second flex circuits.

6. A high-density circuit module comprising:

a first CSP having an upper and a lower major surface and a set of CSP contacts along the lower major surface;

a second CSP having first and second lateral edges and upper and lower major surfaces and a set of CSP contacts along the lower major surface, the first and second lateral edges delineating an extent of the upper major surface of the second CSP;

a form standard disposed above the upper surface of the second CSP; and

a flex circuit.

7. A high-density circuit module comprising:

a first CSP having first and second major surfaces with a plurality of CSP contacts along the first major surface;

a second CSP having first and second major surfaces with a plurality of CSP contacts along the first major surface,

a form standard, the first CSP being disposed above the form standard and the second CSP;

a pair of flex circuits, each of which has first and second conductive layers between which conductive layers there is an intermediate layer, the second conductive layer having demarked a plurality of upper and lower flex contacts and a voltage plane, a first set of said plurality of upper and lower flex contacts being connected to the voltage plane, a second set of said plurality of upper and lower flex contacts being connected to the first conductive layer, and a third set of said plurality of upper and lower flex contacts being comprised of selected ones of upper flex contacts that are connected to corresponding selected ones of lower flex contacts, the plurality of CSP contacts of the first CSP being in contact with the upper flex contacts and the plurality of CSP contacts of the second CSP being in contact with the lower flex contacts; and

a set of module contacts in contact with the lower flex contacts.

8. The high density circuit module of claim 7 in which the first and second CSPs are memory circuits.

9. The high-density circuit module of claim 7 in which:

a data set of the plurality of CSP contacts of the first CSP express an n-bit datapath;

a data set of the plurality of CSP contacts of the second CSP express an n-bit datapath:

each of the flex circuits of the pair of flex circuits has supplemental lower flex contacts which, in combination with the lower flex contacts, provide connection for the set of module contacts and a set of supplemental module contacts to express a 2n-bit module datapath that combines the n-bit datapath expressed by the data set of the plurality of CSP contacts of the first CSP and the n-bit datapath expressed by the data set of the plurality of CSP contacts of the second CSP.

10. The high-density circuit module of claim 7 in which the second set of said plurality of upper and lower flex contacts is connected to the first conductive layer with vias that pass through the intermediate layer.

11. The high-density circuit module of claim 10 in which the second set of said plurality of upper and lower flex contacts is comprised of upper flex contacts connected to the first conductive layer with on-pad vias.

12. The high-density circuit module of claim 10 in which the second set of said plurality of upper and lower flex contacts is comprised of lower flex contacts connected to the first conductive layer with off-pad vias.

13. A memory access system comprising:

a memory expansion board;

a high-density circuit module devised in accordance with claim 6, the high-density circuit module being mounted on the memory expansion board;

a switching multiplexer mounted on the memory expansion board, the switching multiplexer for switching data lines between the first and second integrated circuits; and

a decode logic circuit for decoding chip selection signals from a control circuit and providing a switching multiplexer control signal.

14. A memory access system comprising:

a high-density circuit module devised in accordance with claim 6;

a switch for connecting a datapath to one of the plural integrated circuits of the high-density circuit module;

a decode logic for generating a control signal that causes the switch to connect the datapath to one of the plural integrated circuits in response to a combination signal comprised of a clock signal and a chip select signal.

15. The memory access system of claim 14 in which the plural integrated circuits of the high-density circuit module number four.

16. A memory access system comprising:

plural memory expansion boards each populated with plural high-density circuit modules, each of which plural high-density circuit modules being devised in accordance with claim 6;

plural multiplexers mounted upon each of the plural memory expansion boards, the plural multiplexers for making connections between a datapath and single ones of the plural integrated circuits comprising the high-density circuit modules;

decode logic on each of the plural memory expansion boards, the decode logic for generating a control signal in response to a combination signal comprised of a clock signal and a chip select signal, the control signal causing at least one of the plural multiplexers to connect a particular datapath to a particular one of the plural integrated circuits.

17. The memory access system of claim 16 in which the multiplexers are FET multiplexers.

18. The memory access system of claim 16 in which the plural high-density circuit modules are devised in accordance with claim 1.

19. The memory access system of claim 16 in which the plural high-density circuit modules are comprised of four integrated circuits.

20. The memory access system of claim 16 in which the plural high-density circuit modules are comprised from two integrated circuits.

21. A memory access system comprising:

a memory board having a board memory signal data connection that provides a connection for memory signals between a plurality of integrated circuits mounted on the memory board and memory control circuitry;

a high-density circuit module comprised of first, second, third, and fourth individual integrated circuits, the high-density circuit module being mounted on the memory board and devised in accordance with claim 6;

a switching multiplexer mounted on the memory board, the switching multiplexer having a set of plural input data connections, individual ones of the

plural input data connections connected to provide individual data connections between each of the first, second, third, and fourth individual integrated circuits and the switching multiplexer; and

a decode logic circuit for decoding chip selection signals from a control circuit and providing a switching multiplexer control signal.

22. The memory access system of claim 21 in which the switching multiplexer further comprises an output data connection connected to the board signal memory data connection.

23. The memory access system of claim 22 in which the switching multiplexer provides selective individual connection between the board signal memory data connection and the first, second, third, and fourth individual integrated circuits.

24. The memory access system of claim 23 in which the individual connection between the board signal memory data connection and the first, second, third, and fourth individual integrated circuits occurs in response to the switching multiplexer control signal from the decode logic circuit.

25. The memory access system of claim 21 in which the decode logic circuit is mounted on the memory board.

26. The memory access system of claim 21 in which the high-density memory module is devised in accordance with claim 1.

27. A memory access system comprising:

X memory expansion boards each populated with Y high-density circuit modules devised in accordance with claim 6, each of which Y high-density circuit modules being comprised of Z individual integrated circuits;

plural multiplexers mounted upon each of the X memory expansion boards, the plural multiplexers each for selectively making connections between a datapath and single ones of the Z integrated circuits comprising each of the Y high-density circuit modules;

decode logic on each of the plural memory expansion boards, the decode logic for generating a control signal in response to a combination signal comprised of a clock signal and a chip select signal, the control signal causing at least one of the plural multiplexers to connect a particular datapath to a particular one of the Z integrated circuits.

28. The memory access system of claim 27 in which the multiplexers are FET multiplexers.

29. The memory access system of claim 27 in which the Y high-density circuit modules are devised in accordance with claim 1.

30. The memory access system of claim 27 in which Z equals 4.

31. The memory access system of claim 27 in which Z equals 2.

32. A stacked integrated circuit module comprising:

a base element CSP having upper and lower major surfaces, there being base element contacts along the lower major surface of the base element CSP;

a form standard disposed adjacent to the upper major surface of the base element CSP;

a first support element CSP having upper and lower major surfaces, there being first support element contacts along the lower major surface of the first support element CSP, the first support element CSP being in inverted stacked disposition relative to the base element CSP with its upper major surface adjacent to, but above the form standard so that the form standard is between the base element CSP and the first support element CSP but adjacent to the upper surfaces of both the base element CSP and the first support element CSP;

a flex circuit in contact with the base element contacts of the base element CSP and the first support element contacts while being disposed about the lower surface of the base element CSP, the form standard, and the lower surface of the inverted first support element CSP.

33. The stacked integrated circuit module of claim 32 in which the form standard is affixed to the flex circuit at two different areas of the flex circuit.

34. The stacked integrated circuit module of claim 32 further comprising a second support element CSP having upper and lower major surfaces, there being second support element contacts along the lower major surface of the second support element CSP, the second support element CSP being in inverted stacked disposition relative to the base element CSP with its upper major surface adjacent to, but above the form standard.

35. The stacked integrated circuit of claim 32 in which the form standard is folded over itself.

36. The stacked integrated circuit of claim 34 in which the form standard is affixed to the flex circuit in at least two different areas.

37. A stacked integrated circuit module comprising:

a base element CSP having upper and lower major surfaces;

a form standard disposed adjacent to the upper major surface of the base element CSP;

a support element CSP having upper and lower major surfaces, the support element CSP being in inverted stacked disposition relative to the base element CSP; and

flex circuitry disposed about the base element CSP, the form standard, and the support element CSP so that the base element CSP, the form standard, and the support element CSP are each adjacent to different areas of the flex circuitry.

38. The stacked integration circuit module of claim 37 in which the flex circuitry is affixed to the base element CSP, the form standard, and the support element CSP.

39. The stacked integrated circuit module of claim 37 further comprising a supplemental support element CSP in inverted stacked disposition relative to the base element CSP.

40. The stacked integrated circuit module of claim 37 in which the form standard has a lower radiating portion extending downward outside of a lateral extent of the upper major surface of the base element CSP.

41. The stacked integrated circuit module of claim 37 in which the form standard has a lower radiating portion extending downward outside of a lateral extent of the upper major surface of the base element CSP, and an upper radiating portion extending upward outside of a lateral extent of the upper major surface of the support element CSP.

42. The stacked integrated circuit module of claim 37 in which the form standard has a lower radiating and flex support portion extending downward outside of a lateral extent of the upper major surface of the base element CSP, and an upper radiating and flex support portion extending upward outside of a lateral extent of the upper major surface of the support element CSP, the lower and upper radiating flex support portions each presenting a curved edge about which the flex circuitry is wrapped.

43. A high-density circuit module comprising:

a first CSP having a lower and an upper surface and first and a second edge, the first and second edges delineating a lateral extent for the upper major surface;

a second CSP being in an inverted stacked disposition relative to the first CSP, the second CSP having upper and lower major surfaces;

a form standard disposed between the first and second CSPs, the form standard having a lateral extent greater than the lateral extent of the upper major surface of the first CSP, the form standard having at least one radiating portion extending downward at a location outside the lateral extent of the upper major surface of the first CSP;

a flex circuit connecting the first and second CSPs and disposed to place a first portion of the flex circuit beneath the lower major surface of the first CSP and a second portion of the flex circuit above the second CSP.

44. The high-density circuit module of claim 43 in which the form standard has at least one radiating portion extending upward.

45. The high-density circuit module of claim 43 in which the flex circuit comprises:

first and second conductive layers, between which there is an intermediate layer, the second conductive layer having demarked first and second flex contacts, the first flex contacts in electrical connection with the first CSP and the second flex contacts in electrical connection with the second CSP.

46. The high-density circuit module of claim 43 in which the flex circuit comprises a conductive layer that expresses first and second flex contacts for connection of the first and second integrated circuits respectively.

47. A stacked integrated circuit module comprising:

a base element CSP having upper and lower major surfaces;

a support element CSP having upper and lower major surfaces, the support element CSP being in inverted stacked disposition relative to the base element CSP;

a first form standard disposed adjacent to the upper major surface of the base element CSP, the form standard having an upper radiating portion disposed outside of a lateral extent of the lower major surface of the support element CSP and at least partially beside the support element CSP; and

flex circuitry disposed about the base element CSP, the form standard, and the support element CSP so that the base element CSP, the form standard, and the support element CSP are each adjacent to different areas of the flex circuitry.

48. The stacked integrated circuit module of claim 47 in which the form standard has a lower radiating portion disposed outside of a lateral extent of the upper major surface of the base element CSP and at least partially beside the base element CSP.

49. The high-density circuit module of claim 47 in which the flex circuit comprises:

first and second conductive layers, between which there is an intermediate layer, the second conductive layer having demarked first and second flex contacts, the first flex contacts in electrical connection with the base element CSP and the second flex contacts in electrical connection with the support element CSP.

50. The high-density circuit module of claim 47 in which the flex circuit comprises a conductive layer that expresses first and second flex contacts for connection of the base element CSP and support element CSP.